High Q CMOS-Compatible Microwave Inductors Using Double-Metal Interconnection Silicon Technology

Min Park, Seonghearn Lee, *Member, IEEE*, Hyun Kyu Yu, *Member, IEEE*, Jin Gun Koo, and Kee Soo Nam

***Abstract*— The aim of this letter is to demonstrate the possibility of building high quality factor (Q) integrated inductors in the conventional complementary metal–oxide semiconductor (CMOS) process without any additional processes of previous papers, such as thick gold layer or multilayer interconnection. The comparative analysis is extensively carried out to investigate the detailed variation of Q performance according to inductor shape and substrate by varying the substrate resistivity with circular and rectangular shape. The high Q of nearly 12 is achieved from the fabricated inductors with 2 μm metal thickness on the 2 k$\Omega\cdot$cm silicon substrate using the CMOS process.**

***Index Terms*—Inductor, microwave, silicon technology.**

I. Introduction

WITH THE RAPID growth of wireless communication markets, Si is recognized as a fascinating material to meet the demands of low-cost, high integration, mature technologies [1]. For the silicon radio frequency (RF) integrated circuit (IC) applications, the realization of high quality factor (Q) inductors is important task to be solved imperatively, but this task is confronted with the challenge of microwave performance degradation due to higher substrate losses than GaAs materials [2]. In the early development of inductors on silicon substrate, only a few results have been reported [3], because of the difficulty of obtaining high Q on Si wafers. Recently, Ashby *et al*. described a 2.88-nH inductor with a measured peak Q of 12.1 at 3.3 GHz in a Si bipolar process using a thick gold process and high-resistivity silicon wafer (150 $\sim$ 200 $\Omega\cdot$cm) [4]. At the same time, Burghartz *et al*. reported 1.95-nH inductors with a peak Q of 9.3 at 4 GHz fabricated using the multilevel interconnection metals in BiCMOS technology [2]. It is very difficult and expensive, however, to apply these previous technologies with the conventional Si CMOS process. Thus, it is more attractive to obtain high Q only by increasing the Si substrate resistivity, without any modifications from the existing conventional complementary metal–oxide semiconductor (CMOS) technology.

Manuscript received August 27, 1996. This work was supported by the Ministry of Information and Communication of Korea.

M. Park, H. K. Yu, J. G. Koo, and K. S. Nam are with the Semiconductor Technology Division, Electronics and Telecommunications Research Institute, 161 Kajong-Dong, Yusong-Gu, Taejon 305-350, Korea.

S. Lee is with the Department of Electronic Engineering, Hankuk University of Foreign Studies, Kyungki-do 449-791, Korea.

Publisher Item Identifier S 1051-8207(97)01153-7.

In this letter, spiral inductors with the rectangular and circular shape were built using the conventional CMOS process on Si wafers with various kinds of resistivities in order to investigate the substrate effect on the Q in detail. High Q performance, comparable with a previous result [4], was achieved for the inductors on high-resistivity Si wafers without any complicated or additional process. With this standard CMOS process, f_T of 13 GHz and $f_{\max}$ of 17 GHz was normally obtained for nMOSFET's with the gate length of 0.8 μm.

II. Inductor Fabrication Process

A standard CMOS technology with double-metal TiW/Al-1%Si/TiW interconnects was used to fabricate various inductor structures with rectangular and circular spiral shapes. In this work, geometry dimensions were fixed to be 10 μm width, 2 μm spacing, and inner diameter of 100 μm. Metal layer for inductors was formed by the second metal layer with the total thickness of 1.1 μm, consisting of TiW(75 nm)/Al-1%Si(800 nm)/TiW(220 nm) [5]. Thus, the actual thickness of Al used for CMOS process is much smaller than that for [2] and [4], resulting in higher resistance. Inter-metal dielectrics (IMD's) was deposited with a thickness of 800 nm. The isolating oxide thickness between the first metal and the silicon substrate was about 1.2 μm, the same thickness in the conventional CMOS process. The substrate was grounded to make the inductors operate in CMOS RF IC's. To find the influence of substrate resistivity on the inductor microwave performance, we use three kinds of 625-μm-thick silicon wafers with the low resistivity of 4 $\sim$ 6 $\Omega\cdot$cm, medium resistivity of 30 $\sim$ 50 $\Omega\cdot$cm, and high resistivity of 2 k$\Omega\cdot$cm. To reduce the high metal resistance of our process, the other inductors with TiW/Al-1%Si multilayer metal of 2 μm thickness were fabricated by repeating the second metal process twice.

III. Results and Discussion

Two-port S-parameters were measured on the fabricated inductors using a HP 8510B network analyzer and Cascade Microtech RF probes. The "open" pad patterns without any inductor connections were also measured and used to remove the pad parasitics from measured S-parameters [6]. This pad de-embedding was accurately performed by subtracting Y-parameters of "open" pad pattern from those of the inductors, after the measured S-parameters are converted to

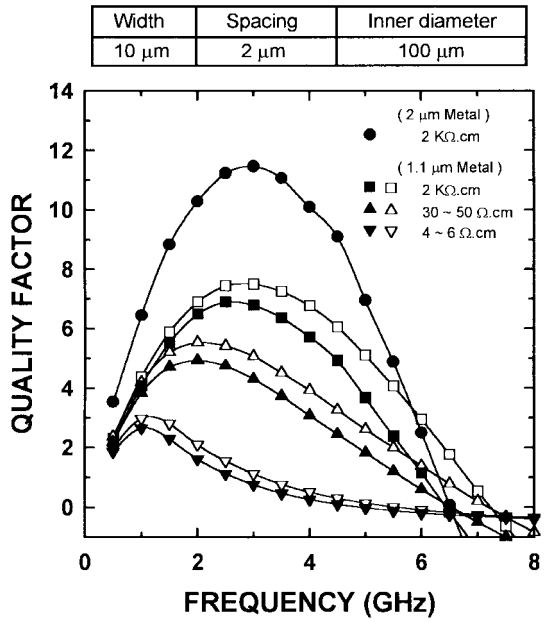

Fig. 1. The quality factor Q of rectangular (filled mark) and circular (open mark) spiral inductors with various kinds of the substrate resistivity as a function of frequency.

Y-parameters. The Q of the inductor was determined as the ratio of the imaginary part to the real part of the one-port input impedance transformed from the measured two-port S-parameters.

Fig. 1 shows the Q values as a function of frequency for rectangular and circular spiral inductors of eight turns fabricated on various kinds of silicon substrate with different resistivity. To inspect the influence of the metal thickness, the Q value of the rectangular spiral inductor with the metal thickness of 2 μm was also compared with these results. The 2-μm metal inductor shows the highest Q with the peak value of the 11.5 at 3.3 GHz, which is nearly comparable with the reported result using gold process [4]. In this figure, Q increases with the frequency up to the peak value and drops at higher frequencies. This is easily understood by the fact that the reactance of input impedance dominated by the inductance at lower frequencies rolls off at higher frequency due to fringing and substrate capacitances.

To describe the variation of Q at different layout and substrate, the lumped equivalent circuit in Fig. 2 has been used. In this circuit, L and R represent the series inductance and resistance, respectively. C_f models the fringing capacitance between the metal lines. C_1 and C_2 represent the capacitance between the metal layer and the grounded substrate, and R_1 and R_2 model the resistance associated with the substrate losses. Model parameters were extracted by fitting the lumped model to the measured S-parameters using HP-EEsof LIBRA. Fig. 2 shows the comparison between the measured and modeled Q for the 2-μm metal inductor on high-resistivity wafer, showing a good agreement. This good agreement verifies the accuracy of the lumped-equivalent circuit for inductors. Note that the degradation of fitting accuracy was found for inductors on low-resistivity wafers, which may results in uncertainties in extracted parameters.

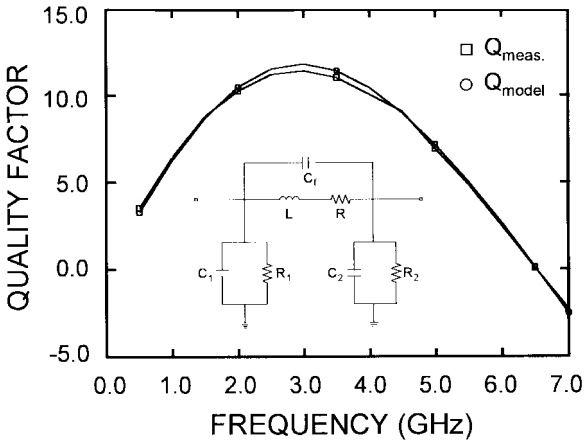

Fig. 2. Measured and modeled Q as a function of frequency using the lumped equivalent circuit shown in this figure for the 2-μm metal inductor.

Table I shows the number of turns (N), maximum value of Q ($Q_{\max}$), the frequency at this Q ($f_{Q\max}$), self-resonant frequency ($f_{\rm res}$), and fitted model parameters for various kinds of fabricated inductors. This information is very useful to explain the frequency response of Q. In Fig. 1, the peak value of Q increases at higher substrate resistivity. This effect is reasonable because of the reduction of R_1 value with decreasing the resistivity of wafer, indicating the rise of substrate conducting losses. Another important observation in Fig. p1 is that the circular spiral inductors have higher peak and broader profile of Q than rectangular inductors. These phenomena can be explained by observing the fact that the circular inductor has a higher ratio of L and R calculated from Table I than the rectangular one.

To observe the physical information of $Q_{\max}$, $f_{Q\max}$, and $f_{\rm res}$ with varying N, the values of $Q_{\max}$, $f_{Q\max}$, and $f_{\rm res}$ are also listed in Table I with modeled parameters. With the increase of N, the values of L and R increase because of longer metal length. However, $Q_{\max}$, $f_{Q\max}$, and $f_{\rm res}$ decrease with increasing N, because of larger total area, which is confirmed by the increase of C_1 and C_f and the decrease of R_1, shown in Table I. This information becomes very useful to choose the proper N in the frequency range of operation of silicon RF IC design for wireless communications.

IV. Conclusion

We fabricated the high Q inductors of the rectangular and circular spiral type on the various kinds of Si substrate with different resistivity and demonstrated the possibility of the high Q inductor designs even in conventional CMOS double-metal interconnection technology. The high Q of nearly 12 is attained for the inductor with 2 μm-metal thickness on the high-resistivity Si wafer of 2 k$\Omega\cdot$cm, using only the CMOS process, which is comparable with previous results using complex Si technology. By modeling these inductors as a lumped circuit, we extensively analyze the effects of substrate resistivity on the frequency dependences of Q and confirm that the substrate losses are dominant factor to determine the Q performance of Si inductors.

TABLE I

SUMMARY OF PERFORMANCE PARAMETERS AND EQUIVALENT CIRCUIT LUMPED-ELEMENT DATA FOR THE VARIOUS KINDS OF SPIRAL INDUCTORS WITH 1.1-μm METAL THICKNESS, EXCEPT FOR HIGH-R(T). THE SYMBOLS USED IN THIS TABLE ARE: HIGH (2 K$\Omega \cdot$ cm); MED (30 $\sim$ 50 $\Omega \cdot$ cm); AND LOW: (4 $\sim$ 6 $\Omega \cdot$ cm) FOR SUBSTRATE TYPE; R (RECTANGULAR) AND C (CIRCULAR) FOR SPIRAL SHAPE; HIGH-R(T) FOR 2 K$\Omega \cdot$ cm SUBSTRATE WITH 2-μm METAL

N	Q_{max}	f_{Qmax} (GHz)	f_{res} (GHz)	L (nH)	R (Ω)	C_f (fF)	C_1 (fF)	C_2 (fF)	R_1 (KΩ)	R_2 (KΩ)	Remark
8	11.5	3.0	6.6	12.98	12.24	24.9	20.9	36.5	11.12	7.98	High-R(T)
8	6.9	3.0	6.3	13.10	19.26	25.6	20.9	37.1	7.11	5.97	High-R
8	4.9	2.0	6.5	13.28	19.51	25.5	19.4	35.4	2.39	1.71	Med-R
8	2.7	1.0	4.7	14.97	17.60	50.1	16.5	55.4	0.37	0.33	Low-R
8	7.5	3.0	7.2	11.90	16.63	22.7	17.5	28.6	6.82	5.06	High-C
8	5.5	2.0	7.1	12.04	16.58	23.1	17.5	28.7	2.60	1.96	Med-C
8	2.7	1.0	4.7	13.18	15.50	41.9	20.9	51.0	0.42	0.40	Low-C
12	4.7	1.5	3.0	34.03	32.49	35.3	40.3	82.4	3.71	1.84	High-R
10	5.7	2.0	4.6	22.05	26.31	31.4	26.2	52.7	5.49	3.26	High-R
8	6.9	3.0	6.3	13.10	19.26	25.6	20.9	37.1	7.11	5.97	High-R
6	7.9	4.0	10.2	6.84	13.06	18.0	15.5	23.0	6.63	5.57	High-R
4	13.3	10.5	14.5	2.85	7.87	9.0	12.6	14.8	12.26	18.78	High-R

* Fixed at metal width = 10 μm, metal spacing = 2 μm, inner diameter of inductor = 100 μm.

ACKNOWLEDGMENT

The authors would like to thank S. J. An for his technical assistance with S-parameter measurements. They also appreciate the assistance from all members of Silicon RF Device Research Group at ETRI.

REFERENCES

[1] N. Camiller, J. Costa, D. Lovelace, and D. Ngo, "Silicon MOSFET's, the microwave device technology for the 90s," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1993, pp. 545–548.

[2] J. N. Burghartz, M. Soyuer, and K. A. Jenkins, "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 100–104, Jan. 1996.

[3] N. M. Nguyen and R. G. Meyer, "Si IC-compatible inductors and LC passive filters," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1028–1031, Aug. 1990.

[4] K. B. Ashby, I. A. Koullias, W. C. Finley, J. J. Bastek, and S. Moinian, "High Q inductors for wireless applications in a complementary silicon bipolar process," *IEEE J. Solid-State Circuits*, vol. 31, pp. 4–9, Jan. 1996.

[5] M. Park, G. H. Kim, J. M. Park, S. G. Kim, Y. C. Hyeon, J. G. Koo, and K. S. Nam, "Multilevel interconnection technology using new pillar formation method and CMP planarization," in *Proc. IEEE CMP-MIC Conf.*, Santa Clara, CA, 1996, pp. 291–298.

[6] P. J. van Wijnen, H. R. Claessen, and E. A. Wolsheimer, "A new straightforward calibration and correction procedure for 'on wafer' high-frequency S-parameter measurements (45 MHz-18 GHz)," in *IEEE Bipolar Circuits and Technol. Meet.*, 1987, pp. 70–73.